IN THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) A method of operating a memory device, comprising:

receiving an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals, wherein the set of command and address signals consists of an Active command, Bank Address signals, and Row Address signals, and wherein receiving the F-bit word comprises:

receiving a first portion of the F-bit word substantially simultaneous with receiving a first edge of a clock signal, wherein the first portion of the F-bit word comprises G-bits, wherein G is less than F, wherein the G-bit portion comprises a first subset of [[a]] the set of command and address signals; and

receiving a second portion of the F-bit word substantially simultaneous with receiving a second edge of the clock signal, wherein the second portion of the F-bit word comprises H-bits, wherein H is F-G, wherein the H-bit portion comprises a second subset of the set of command and address signals; and

performing a memory command in response to the received F-bit word.

2. (Previously Presented) The method of claim 1, wherein the memory device comprises a device selected from the group consisting of a DRAM device, a static random access memory (SRAM) device, and a static memory device.

3. (Previously Presented) The method of claim 1, further comprising:

sending the first portion of the F-bit word substantially simultaneous with sending the first edge of the clock signal by an external controller; and

sending the second portion of the F-bit word substantially simultaneous with sending the second edge of the clock signal by the external controller.

4. (Original) The method of claim 3, wherein, in sending, the external controller is a device selected from the group consisting of a DRAM controller, a central processing unit (CPU), a graphics processing unit (GPU), and a processor.

5. (Currently Amended) A method of operating a memory device, comprising:

receiving an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals, wherein the set of command and address signals consists of an Active command, Bank Address signals, and Row Address signals, and wherein receiving the F-bit word comprises:

receiving a first portion of the F-bit word substantially simultaneous with receiving a first edge of a clock signal, wherein the first portion of the F-bit word comprises G-bits, wherein G is less than F, wherein the G-bit portion comprises a set of command signals and a first subset of a set of address signals; and

receiving a second portion of the F-bit word substantially simultaneous with receiving a second edge of the clock signal, wherein the second portion of the F-bit word comprises H-bits, wherein H is F-G, wherein the H-bit portion comprises a second subset of the set of address signals; and

performing a memory command in response to the received F-bit word.

6. (Previously Presented) The method of claim 5, wherein the memory device comprises a device selected from the group consisting of a DRAM device, a static random access memory (SRAM) device, and a static memory device.

7. (Original) The method of claim 5, wherein the first and second edges of the clock signal comprise rising and falling edges of the clock signal, wherein in the rising and falling edges comprise a transition from a logic level "zero" to a logic level "one" and a transition from the logic level "one" to the logic level "zero", respectively.

8. (Currently Amended) A method of operating a memory device, comprising:

receiving an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals, wherein the set of command and address signals consists of an Active command, Bank Address signals, and Row Address signals, and wherein receiving the F-bit word comprises:

receiving a first portion of the F-bit word substantially simultaneous with receiving a first edge of a first cycle of a clock signal, wherein the first portion of the F-bit word comprises G-bits, wherein G is less than F, wherein the G-bit portion comprises a first subset of a set of command and address signals; and

receiving a second portion of the F-bit word substantially simultaneous with receiving a first edge of a second cycle of the clock signal, wherein the second portion of the F-bit word comprises H-bits, wherein H is F-G, wherein the H-bit portion comprises a second subset of the set of command and address signals; and

performing a memory command in response to the received F-bit word.

9. (Previously Presented) The method of claim 8, wherein, in receiving the second portion of the F-bit word, the second cycle is substantially subsequent to the first cycle.

10. (Previously Presented) The method of claim 8, wherein the memory device comprises a device selected from the group consisting of a DRAM device, a static random access memory (SRAM) device, and a static memory device.

11. (Currently Amended) A method of operating a memory device, comprising:

receiving an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals, wherein the set of command and address signals consists of an Active command, Bank Address signals, and Row Address signals, and wherein receiving the F-bit word comprises:

receiving a first portion of the F-bit word substantially simultaneous with receiving a first edge of a first cycle of a clock signal, wherein the first portion of the F-bit word comprises G-bits, wherein G is less than F, wherein the G-bit portion comprises a set of command signals and a first subset of a set of address signals; and

receiving a second portion of the F-bit word substantially simultaneous with receiving a first edge of a second clock cycle of the clock signal, wherein the second portion of the F-bit word comprises H-bits, wherein H is F-G, wherein the H-bit portion comprises a second subset of the set of address signals; and

performing a memory command in response to the received F-bit word.

12. (Previously Presented) The method of claim 11, wherein, in receiving the second portion of the F-bit word, the second cycle is substantially subsequent to the first cycle.

13. (Previously Presented) The method of claim 11, wherein a clock signal comprises a first and second edge, wherein the first and second edges of the clock signal comprise rising and falling edges of the clock signal, wherein in the rising and falling edges comprise a transition from a logic level "zero" to a logic level "one" and a transition from the logic level "one" to the logic level "zero", respectively.

14. (Previously Presented) The method of claim 11, wherein the memory device comprises a device selected from the group consisting of a DRAM device, a static random access operating memory (SRAM) device, and a static memory device.

15-17. (Canceled)

18. (Currently Amended) A memory device comprising:

multiple command and address pins to receive a first portion of an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals, wherein the set of command and address signals consists of an Active command, Bank Address signals, and Row Address signals, wherein the first portion of the F-bit word comprises a first subset of the set of command and address signals, wherein the multiple command and address pins receive the first portion of the F-bit word substantially simultaneous with receiving a first edge of a first cycle of a clock signal, wherein the multiple command and address pins to further receive a second portion of an F-bit word, wherein the second portion of the F-bit word comprises a second subset of the set of command and address signals, wherein the multiple command and address pins receive the second portion of the F-bit word substantially simultaneous with receiving a first edge of a second cycle of the clock signal, and wherein the memory device to perform a memory command in response to the received F-bit word.

19. (Previously Presented) The memory device of claim 18, wherein the memory device is a device selected from the group consisting of a DRAM device, a static random access memory (SRAM) device, and a static memory device.

20. (Previously Presented) The memory device of claim 18, wherein a clock signal comprises a first and second edge, wherein the first and second edges of the clock signal comprise rising and falling edges of the clock signal, respectively, wherein in the rising and falling edges comprise a transition from a logic level "zero" to a logic level "one" and a transition from the logic level "one" to the logic level "zero", respectively.

21-23. (Canceled)

24. (Currently Amended) A memory circuit comprising:

one or more integrated circuit memory devices operable for sending and receiving signals, wherein each of the integrated circuit memory devices operates to receive a first portion of an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals, wherein the set of command and address signals consists of an Active command, Bank Address signals, and Row Address signals, wherein the first portion of the F-bit word comprises a first subset of the set of command and address signals, wherein ~~the multiple command and address pins~~ each of the integrated circuit memory devices operates to receive the first portion of the F-bit word substantially simultaneous with receiving a first edge of a first cycle of a clock signal, wherein each of the integrated memory circuit devices operates to further receive a second portion of an F-bit word, wherein the second portion of the F-bit word comprises a second subset of the set of command and address signals, wherein ~~the multiple command and address pins~~ each of the integrated circuit memory devices operates to receive the second portion of the F-bit word substantially simultaneous with receiving a first edge of a second cycle of the clock signal, and wherein each integrated circuit memory device operates to perform a memory command in response to the received F-bit word.

25. (Previously Presented) The memory circuit of claim 24, wherein the second cycle is substantially subsequent to the first cycle in the clock signal.

26. (Previously Presented) The memory circuit of claim 24, wherein a clock signal comprises a first and second edge, wherein the first and second edges of the clock signal comprise rising and falling edges of the clock signal, respectively, wherein in the rising and falling edges comprise a transition from a logic level "zero" to a logic level "one" and a transition from the logic level "one" to the logic level "zero", respectively.

27. (Previously Presented) The memory circuit of claim 24, wherein the integrated circuit memory device is a memory device selected from the group consisting of a DRAM device, a SRAM device, and a static memory device.

28-38. (Canceled)

39. (Previously Presented) The method of claim 1, wherein the integrated circuit memory device is a volatile memory device.

40. (Previously Presented) The method of claim 5, wherein the integrated circuit memory device is a volatile memory device.

41. (Previously Presented) The method of claim 8, wherein the integrated circuit memory device is a volatile memory device.

42. (Previously Presented) The method of claim 11, wherein the integrated circuit memory device is a volatile memory device.

43. (Canceled)

44. (Previously Presented) The memory device of claim 18, wherein the integrated circuit memory device is a volatile memory device.

45. (Canceled)

46. (Previously Presented) The memory circuit of claim 24, wherein the integrated circuit memory device is a volatile memory device.

47-48. (Canceled)

49. (Currently Amended) A method, comprising:

receiving an F-bit word using J command and address pins of a programmable memory device, wherein F and J are positive integers, wherein J is less than F, wherein the F-bit word comprises a set of command and address signals, and wherein the set of command and address signals consists of an Active command, Bank Address signals, and Row Address signals, comprising:

receiving a first portion of the F-bit word at a first time using G command and address pins, wherein the first portion of the F-bit word comprises G-bits, wherein G is less than F, wherein G is less than or equal to J, [[and]] wherein the first portion of the F-bit word consists of ~~command and address signals~~ a set of command signals and a first subset of address signals, wherein the set of command signals includes a Chip Select (CS#) signal, a Row Address Strobe (RAS#) signal, a Column Address Strobe (CAS#) signal, and a Write Enable (WE#) signal, wherein receiving the set of command signals includes using a set of Command Pins, wherein the set of Command Pins include a CS# pin, a RAS# pin, a CAS# pin, and a WE# pin, wherein receiving the first subset of address signals includes using a set of Address Pins, and wherein the set of Address Pins include G-4 pins; and

receiving a second portion of the F-bit word at a second time, wherein the second portion of the F-bit word comprises H-bits, wherein H is F-G, wherein H is less than or equal to J, and wherein the second portion of the F-bit word consists of ~~command and address signals~~ a second subset of address signals; and

performing a memory command in response to the fully-received F-bit word.

50. (Previously Presented) The method of claim 49, wherein a first time includes at or substantially simultaneously with receiving a first edge of a clock signal.

51. (Previously Presented) The method of claim 50, wherein the first edge of a clock signal includes a first edge of a first cycle of the clock signal.

52. (Previously Presented) The method of claim 51, wherein the first edge is a rising edge of the clock signal.

53. (Currently Amended) The method of claim [[52]] 51, wherein the first edge is a falling edge of the clock signal.

54. (Previously Presented) The method of claim 49, wherein a second time includes at or substantially simultaneously with receiving a second edge of a clock signal.

55. (Previously Presented) The method of claim 54, wherein the second edge of a clock signal includes a first edge of a second cycle of the clock signal.

56. (Previously Presented) The method of claim 55, wherein the second edge is a rising edge of the clock signal.

57. (Currently Amended) The method of claim [[56]] 55, wherein the second edge is a falling edge of the clock signal.

58-64. (Canceled)

65. (Currently Amended) The method of claim 49, wherein [[a]] the programmable memory device includes a device selected from the group consisting of a dynamic random access memory (DRAM) device, a static random access memory (SRAM) device, and a static memory device.

66. (Currently Amended) The method of claim 49, wherein [[a]] the programmable memory device includes a volatile memory device.

67. (Previously Presented) The method of claim 49, further comprising:
sending the first portion of the F-bit word with a controller at a first time; and
sending the second portion of the F-bit word with a controller at a second time.

68. (Currently Amended) The method of claim 67, wherein [[a]] the controller is a device selected from the group consisting of a DRAM controller, a central processing unit (CPU), a graphics processing unit (GPU), and a processor.

69. (Currently Amended) The method of claim 67, wherein [[a]] the first time includes at or substantially simultaneously with receiving a first edge of a clock signal.

70. (Previously Presented) The method of claim 69, wherein the first edge of a clock signal includes a first edge of a first cycle of the clock signal.

71. (Previously Presented) The method of claim 70, wherein the first edge is a rising edge of the clock signal.

72. (Currently Amended) The method of claim [[71]]70, wherein the first edge is a falling edge of the clock signal.

73. (Currently Amended) The method of claim 67, wherein [[a]] the second time includes at or substantially simultaneously with receiving a second edge of a clock signal.

74. (Previously Presented) The method of claim 73, wherein the second edge of a clock signal includes a first edge of a second cycle of the clock signal.

75. (Previously Presented) The method of claim 74, wherein the second edge is a rising edge of the clock signal.

76. (Currently Amended) The method of claim [[75]] 74, wherein the second edge is a falling edge of the clock signal.

77. (Previously Presented) The method of claim 49, wherein H and G are not equal to each other.

78. (Currently Amended) The method of claim 49, wherein [[a]] the programmable memory device consists of J command and address pins.

79. (Canceled)

80. (New) The method of claim 49, wherein the set of address signals comprises Bank Address signals BA0-BA2 and Row Address signals A0-A11.

81. (New) The method of claim 49, wherein the set of command and address signals consists of an Active command signal, Bank Address signals BA0-BA2, and Row Address signals A0-A11.

82. (New) The method of claim 49, wherein receiving the Active command signal comprises receiving CS# low, RAS# low, CAS# high, and WE# high.

83. (New) The method of claim 49, wherein receiving the second subset of address signals includes using at least one of the set of Address Pins.

84. (New) The method of claim 49, wherein receiving the second subset of address signals includes using at least one Command Pin and at least one Address Pin.

85. (New) The method of claim 84, wherein using the at least one Command Pin and the at least one Address Pin include using H command and address pins, wherein H is greater than G-4.

86. (New) The method of claim 84, wherein the at least one Command Pin includes the RAS# pin.

87. (New) The method of claim 84, wherein the at least one Command Pin includes the CAS# pin.

88. (New) The method of claim 84, wherein the at least one Command Pin includes the WE# pin.

89. (New) The method of claim 49, wherein J is not a multiple of F.

90. (New) A method, comprising:

receiving a set of command and address signals using J command and address pins of a programmable memory device, wherein J is a positive integer, wherein J is less than the number of command and address signals, comprising:

receiving a first portion of the set of command and address signals at a first time using G command and address pins, wherein the first portion of the set of command and address signals comprises G-bits, wherein G is less than the number of command and address signals, wherein G is less than or equal to J, wherein the first portion of the set of command and address signals consists of a set of command signals and a first subset of address signals, wherein the set of command signals includes a Chip Select (CS#) signal, a Row Address Strobe (RAS#) signal, a Column Address Strobe (CAS#) signal, and a Write Enable (WE#) signal, wherein receiving the set of command signals includes using a set of Command Pins, wherein the set of Command Pins include a CS# pin, a RAS# pin, a CAS# pin, and a WE# pin, wherein receiving the first subset of address signals includes using a set of Address Pins, and wherein the set of Address Pins includes G-4 pins; and

receiving a second portion of the set of command and address signals at a second time, wherein the second portion of the set of command and address signals comprises H-bits, wherein H is the number of command and address signals minus G, wherein H is less than or equal to J, wherein the second portion of the set of command and address signals consists of a second subset of address signals, and wherein receiving the second subset of address signals includes using at least one Command Pin and at least one Address Pin; and

performing a memory command in response to the fully-received F-bit word.

91. (New) The method of claim 90, wherein J is not a multiple of F.

92. (New) A method, comprising:

receiving an Active command signal, Bank Address signals, and Row Address signals using command and address pins of a programmable memory device, comprising:

receiving the Active command signal, the Bank Address signals, and a first subset of the Row Address signals at a first time using the command and address pins, wherein the Active command signal includes a Chip Select (CS#) low signal, a Row Address Strobe (RAS#) low signal, a Column Address Strobe (CAS#) high signal, and a Write Enable (WE#) high signal, wherein the CS# signal is received using a CS# command pin, wherein the RAS# signal is received using a RAS# command pin, wherein the CAS# signal is received using a CAS# command pin, and wherein the WE# signal is received using a WE# command pin, wherein the Bank Address signals include BA0-BA2 signals, wherein the BA0 signal is received using a BA0 address pin, wherein the BA1 signal is received using a BA1 address pin, and wherein the BA2 signal is received using a BA2 address pin, and wherein the first subset of Row Address signals includes A11-A9 signals, wherein the A11 signal is received using a A11 address pin, wherein the A10 signal is received using a A10 address pin, and wherein the A9 signal is received using a A9 address pin; and

receiving a second subset of the Row Address signals at a second time using the command and address pins, wherein the second subset of Row Address signals includes A8-A0 signals, wherein the A8 signal is received using the RAS# pin, wherein the A7 signal is received using the CAS# pin, wherein the A6 signal is received using the WE# pin, wherein the A5 signal is received using the BA0 pin, wherein the A4 signal is received using the BA1 pin, wherein the A3 signal is received using the BA2 pin, wherein the A2 signal is received using the A11 pin, wherein the A1 signal is received using the A10 pin, and wherein the A0 signal is received using the A9 pin; and

performing a memory command in response to the fully-received Active command signal, Bank Address signals, and Row Address signals.

93. (New) The method of claim 90, wherein J is not a multiple of F.

94. (New) A method, comprising:

receiving an Active command signal, Bank Address signals, and Row Address signals using command and address pins of a programmable memory device, comprising:

receiving the Active command signal, the Bank Address signals, and a first subset of the Row Address signals at a first time using the command and address pins, wherein the Active command signal includes a Chip Select (CS#) low signal, a Row Address Strobe (RAS#) low signal, a Column Address Strobe (CAS#) high signal, and a Write Enable (WE#) high signal, wherein the CS# signal is received using a CS# command pin, wherein the RAS# signal is received using a RAS# command pin, wherein the CAS# signal is received using a CAS# command pin, and wherein the WE# signal is received using a WE# command pin, wherein the Bank Address signals include BA0-BA2 signals, wherein the BA0 signal is received using a BA0 address pin, wherein the BA1 signal is received using a BA1 address pin, and wherein the BA2 signal is received using a BA2 address pin, and wherein the first subset of Row Address signals includes A12-A8 signals, wherein the A12 signal is received using a A12 address pin, wherein the A11 signal is received using a A11 address pin, wherein the A10 signal is received using a A10 address pin, wherein the A9 signal is received using a A9 address pin, and wherein the A8 signal is received using a A8 address pin; and

receiving a second subset of the Row Address signals at a second time using the command and address pins, wherein the second subset of Row Address signals includes A7-A0 signals, wherein the A7 signal is received using the BA0 pin, wherein the A6 signal is received using the BA1 pin, wherein the A5 signal is received using the BA2 pin, wherein the A4 signal is received using the A12 pin, wherein the A3 signal is received using the A11 pin, wherein the A2 signal is received using the A10 pin, wherein the A1 signal is received using the A9 pin, and wherein the A0 signal is received using the A8 pin; and

performing a memory command in response to the fully-received Active command signal, Bank Address signals, and Row Address signals.

95. (New) The method of claim 90, wherein J is not a multiple of F.